Abstracts

Over-60-GHz design technology for an SCFL dynamic frequency divider using InP-based HEMTs

Y. Umeda, K. Osafune, T. Enoki, H. Yokoyama, Y. Ishii and Y. Imamura. "Over-60-GHz design technology for an SCFL dynamic frequency divider using InP-based HEMTs." 1998 Transactions on Microwave Theory and Techniques 46.9 (Sep. 1998 [T-MTT]): 1209-1214.

A toggle operation of 39-63.5 GHz without tuning has been achieved by a digital dynamic frequency divider (DFD). The DFD employs a pair of clocked inverters (CIs) with source-coupled FET logic (SCFL) and uses 0.1-/spl mu/m-gate InAlAs/InGaAs/InP high electron-mobility transistors (HEMTs) of good uniformity and high performance. On a 2-in wafer, the frequency divider showed a maximum toggle frequency (f/sub tog,max/) of 59.1/spl plusmn/3.3 GHz and a fabrication yield of 89%. This is the highest operation frequency ever reported for a broad-band digital frequency divider. Comparison of the DFD and the static frequency divider (SFD) showed that the ratio of f/sub tog,max/ for the DFD to that for the SFD is much higher than the value expected from the linear-response theory. The comparison also showed that the ratio of the measured f/sub tog,max/ for the DFD to that for the SFD is 1.7, in contrast with the value of two expected from the circuit simulation. Delay-time analysis revealed that this 15% decrease of the ratio is due to the transmission delay of interconnections and charging time for stray capacitance.

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